Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT A**
2. **INPUT A**
3. **OUTPUT A**
4. **INPUT B**
5. **INPUT B**
6. **OUTPUT B**
7. **GND**
8. **OUTPUT C**
9. **INPUT C**
10. **INPUT C**
11. **OUTPUT D**
12. **INPUT D**
13. **INPUT D**
14. **VCC**

**.035”**

**2 3 4 5**

**12**

**13**

**14**

**1**

**8**

**7**

**6**

**11 10 9**

**.038”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref: 0266**

**APPROVED BY: DK DIE SIZE .035” X .038” DATE: 8/30/21**

**MFG: ST MICRO / SIGNETICS THICKNESS .015” P/N: 54LS00**

**DG 10.1.2**

#### Rev B, 7/1